

APPENDIX A

Marked Up Version of Amended Paragraphs

Page 2 lines 15-21:

Fig. 1 illustrates a substrate **102** and a pair of FETs **104a**, **104b**, each including a gate electrode **106** disposed over a gate dielectric layer **107**, and further including source/drain regions **112**. FETs **104a**, **104b** also have conventional sidewall spacers formed from layers [The spacers include a first layer **106** and a second layer] **108** as shown. When a dielectric layer **114** of phosphorous doped glass is formed over substrate **102** and FETs **104a**, **104b**, a void **116** develops as a result of the narrow spacing between FETs **104a**, **104b**.

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Fig. 3 shows a portion of a partially processed wafer having gate electrodes **106** disposed over gate dielectric layers **107**, with gate dielectric layers **107** disposed, in turn, on the surface of a substrate **102**. Tip regions (sometimes referred to as source/drain extensions) **302** are disposed in substrate **102** in alignment with gate electrodes **106**. [This] Those skilled in this field will recognize that these tip regions are generally formed by ion implantation, and that the material implanted is of a conductivity type opposite the conductivity type of substrate **102**. Gate electrodes **106**, gate dielectrics **107**, and tip regions **302**, may be formed by conventional well-known methods.